What is claimed is:

1. A semiconductor integrated circuit, comprising:

a plurality of flip-flop circuits being operated by a clock signal for normal operation during a normal operation, respectively, and configuring a scan chain to be operated by a clock signal for scan during a scan test;

a clock circuit for normal operation for transmitting said clock signal for normal operation to said flip-flop circuit;

a clock circuit for scan for transmitting said clock signal for scan to said flip-flop circuit,

wherein said clock circuit for scan has a lattice-shaped wiring portion, and supplies said clock signal for scan taken out of said lattice-shaped wiring portion to said flip-flop circuit.

2. The semiconductor integrated circuit according to claim 1, wherein the flip-flop circuits are arranged in the interior and the neighborhood region of the lattice-shaped wiring portion of the clock circuit for scan, and wherein said clock circuit for scan has a external clock input terminal for scan for inputting the clock signal for scan, inputs the clock signal for scan which is transmitted from said external clock input terminal for scan to the center of said lattice-shaped wiring portion, and takes out the clock signal for scan from a predetermined location of said lattice-shaped wiring portion,

respectively, to supply it to each said flip-flop circuit.

3. The semiconductor integrated circuit according to claim 1, wherein a selector circuit is arranged to each flip-flop circuit, and wherein said selector circuit inputs the clock signal for normal operation which is transmitted through the clock circuit for normal operation and the clock signal for scan which is transmitted through the clock circuit for scan, selects said clock signal for normal operation during the normal operation to output it to said flip-flop circuit, and selects said clock signal for scan during the scan test to output it to said flip-flop circuit.

4. The semiconductor integrated circuit according to claim 1, wherein the clock circuit for normal operation is configured so that transmission paths of the clock signal for normal operation may become in a tree-shape.

5. The semiconductor integrated circuit according to claim 1, wherein there are a plurality of types of clock signals for normal operation which are transmitted through the clock circuit for normal operation, and any one type of said clock signals for normal operation among the plurality of types thereof is supplied to each flip-flop circuit which configures the scan chain and said clock signal for normal operation of the same type is supplied to said flip-flop circuits which synchronize during the normal operation, and wherein said clock circuit for normal operation is configured so that transmission

paths of the clock signal for normal operation for each type may become in the tree-shape.

6. The semiconductor integrated circuit according to claim 1, wherein the clock circuit for scan has a external clock input terminal for scan for inputting the clock signal for scan, and connects the driver element which drives said lattice-shaped wiring portion between said external clock input terminal for scan and the lattice-shaped wiring portion, and

wherein a power supply wiring of said driver element is wider in width and has a lower resistance compared with a power supply wiring of an element which configures the clock circuit for normal operation.

7. The semiconductor integrated circuit according to claim 1, wherein the clock circuit for scan has a external clock input terminal for scan to which the clock signal for scan is inputted, and connects the driver element which drives said lattice-shaped wiring portion between said external clock input terminal for scan and the lattice-shaped wiring portion, and

wherein the power supply voltage of said driver element is made lower than the power supply voltage of the element which configures the clock circuit for normal operation.

8. The semiconductor integrated circuit according to claim 1, wherein the clock circuit for scan has a external clock input terminal for scan for inputting the clock signal for scan, and connects the driver element which drives said

lattice-shaped wiring portion between said external clock input terminal for scan and the lattice-shaped wiring portion, and

wherein a scan chain connection is performed from a flip-flop circuit, whose shortest transmission path from said driver element of the clock signal for scan which is transmitted to each flip-flop circuit via said lattice-shaped wiring portion from said driver element is longer, towards a flip-flop circuit, whose shortest transmission path is shorter.

9. The semiconductor integrated circuit according to claim 1, wherein a part of the wiring used as the transmission path of the clock signal for normal operation of the clock circuit for normal operation is arranged in parallel with the wiring of the lattice-shaped wiring portion of the clock circuit for scan, a signal which is fixed to the ground potential is used in place of the clock signal for scan during the normal operation, and the signal which is fixed to the ground potential is used in place of the clock signal for normal operation during the scan test.